REMARKS

Favorable consideration of this application is respectfully requested.

Claims 1-23 are currently active in this case.

In the outstanding Official Action Claims 1-23 were rejected under 35 USC 102(b) as being anticipated by *Dupenloup* (US Patent No. 6,205,572).

Applicants respectfully traverse the rejection of Claim 1 under 35 USC 102(b) as being anticipated by *Dupenloup*. Claim 1 recites:

> ***1. A method for synthesizing an integrated circuit design, the method comprising:***
> ***performing physical optimization of block and wire placement, before performing logic synthesis;***
> ***partitioning the blocks into cores and shells;***
> ***synthesizing the shells and cores; and***
> ***recombining the cores and shells into blocks.***

However, *Dupenloup* fails to teach or suggest the same subject matter.

Applicants respectfully traverse the assertion in the outstanding Office Action that equates discussion in *Dupenloup* (e.g., at col 10, ll.8-22, and col 15, ll.20-47), regarding modules/sub-modules and combinational logic/output being registered or driven by a flip-flop, as being comparable or teaching Applicants' claimed *"partitioning the blocks into cores and shells."*

Applicants admit that *Dupenloup* Discusses partitioning of a design into modules of lower complexity (*Dupenloup*, col 10. Line 9). However, modules or blocks are generally known to be portions of circuits containing a set of discrete inputs, outputs, and related logic. Sub-modules are generally known to be blocks within a module (or blocks within blocks), that are generally utilized to break the design into more fundamental components. In contrast, shells and cores are

portions of a block that not only break a design into components, but also meet specific definitional requirements. Primarily, those definitional requirements, as elaborated on in Applicants' specification, define a core as the logic in a block bounded by registers, and a shell as the logic between a core and the pins of the block (e.g., see Applicants' specification page 8, lines 16-18). However, *Dupenloup* gives no consideration to shells and cores as defined by Applicants.

Therefore, even if Applicants' claimed shells and cores are appropriately considered sub-blocks, *Dupenloup* still fails to teach or suggest Applicants' claimed invention because the blocks and sub-blocks of *Dupenloup* only define a broader category that generically describes any hierarchical breakdown of a circuit into its component groups.

Applicants admit that *Dupenloup* goes further to describe certain modules/submodules as being pure down to leaf modules (col. 15, line 23). For example, Dunloup's discussion of modules without impure hierarchical mixtures having (e.g., containing only logic circuits). However, such circuits do not equate to Applicants' defined cores and shells. Therefore, *Dupenloup* fails to describe blocks and/or sub-blocks that meet Applicants' shell and core definition (Claim 1 requires the partitions be made via shells and cores, not simply the broader blocks and/or sub-blocks, or sub-blocks that are pure or logic only circuits as described in *Dupenloup*).

Applicants respectfully traverse any assertion that would equate registration of outputs (driven by flip-flops, col. 15, ll. 37-47) to any part of Applicants' *"partitioning the blocks into shells and cores."* Primarily, the registration of outputs or use of flip flops to drive outputs (and/or any separate compilation of modules having registered outputs) is not the same as partitioning a block into cores and shells.

Applicants also respectfully traverse any assertion that would equate *Dupenloup's* further statements regarding extraction of logic that surrounds memories (col. 15, ll. 58-60) as teaching any part of Applicants' claimed invention. In particular, Applicants respectfully note that, as defined in Applicants' specification, shell and core partitioning is performed on logic between memory elements and logic before or after a memory element in a block. That *Dupenloup* might teach extracting logic that surrounds a memory only suggests an extraction of the logic, but does not teach or suggest a partitioning of the block into cores and shells.

Therefore, Applicants respectfully submit that Claim 1 cannot be anticipated by *Dupenloup* because *Dupenloup* fails to teach or suggest subject matter specifically claimed in Claim 1. Accordingly, Applicants respectfully submit that Claim 1 is patentable over *Dupenloup.*

Applicants also respectfully traverse the rejection of Claims 8 under 35 USC 102(b) as being anticipated by *Dupenloup*. Claim 8 recites:

> ***8. A method for designing deep sub-micron integrated circuits, the method comprising:***
> ***performing layout of physical blocks by estimating an area for each block;***
> ***connecting pins of the blocks with no timing constraints;***
> ***assigning each wire to a metal layer pair;***
> ***optimizing the speed of each wire for its respective layer;***
> ***partitioning the blocks into cores and shells;***
> ***synthesizing the shells;***
> ***synthesizing the cores; and***
> ***recombining the shells and cores.***

However, *Dupenloup* fails to teach or suggest the same subject matter.

Applicants respectfully note Claim 8's inclusion of the step of ***"partitioning the blocks into cores and shells"*** which, similar to the above discussion is neither taught or suggested by *Dupenloup*.

Further, Applicants respectfully note the recited limitation of ***"connecting pins of the blocks with no timing constraints."*** Applicants respectfully traverse any assertion that would rely on *Dupenloup* to suggest the same. For example, at the cited paragraphs (col. 79, ll. 63-67 and col 80, ll.1-11), *Dupenloup* does not suggest that no timing constraints are utilized during either the global routing or detailed routing phases.

Therefore, based on each of the above discussions, Applicants respectfully submit that Claim 8 cannot be anticipated by *Dupenloup*. Because *Dupenloup* fails to teach or suggest several pieces of subject matter specifically claimed in Claim 8. Accordingly, Applicants respectfully submit that Claim 8 is patentable over *Dupenloup*.

Applicants also respectfully traverse the rejections of Claims 13 and 17 under 35 USC 102(b) as being anticipated by *Dupenloup*. Applicants respectfully note that Claims 13 and 17 include the following limitations:

Claim 13: *"partitioning each block into a core and a shell."*

Claim 17: *"partitioning the blocks into cores and shells."*

Applicants also respectfully note that each of the above limitations describe a process, or step therein, not taught or suggested by *Dupenloup.* In particular, Applicants respectfully note the above discussion on a similar topic with respect to Claim 1. Therefore, Applicants respectfully submit that each of Claims 13, and 17 are also patentable over *Dupenloup*.

Based on the patentability of independent Claims 1, 8, 13, and 17, Applicants further respectfully submit that dependent Claims 2-7, 9-12, 14-16, and 18-23 are also patentable.

Applicants respectfully request consideration of dependent Claims 10. Claim 10 recites:

> ***10. The method of Claim 9, wherein optimizing the speed of each wire comprises minimizing a delay in each wire by inserting buffers at optimal distances.***

Therefore, in addition to the patentably distinguishing limitations present in parent Claim 1, Claim 10 includes that the optimization of each wire comprise ***"minimizing a delay in each wire by inserting buffers at optimal distances"*** However, *Dupenloup* fails to teach or suggest the same.

Applicants respectfully traverse the assertion in the outstanding Office Action that equates *Dupenloup's* use of buffers to solve fan in/out problems by inserting buffers (e.g., col. 41, lines 10-27). Applicants respectfully note that inserting buffers to solve fan-in/out problems is well known. However, as claimed, Applicants' insertion of buffers is done to minimize delay, and therefore requires the claimed buffer insertion at optimal distances. However, *Dupenloup* inserts buffers to solve violations caused by a high fanout ratio of the circuit, and makes no suggestion of inserting buffers at optimal distances to minimzie delay.

Applicants respectfully note that *Dupenloup* provides some discussion of using buffers to balance clock trees (e.g., col. 11, lines 5-7). However, buffer insertion to balance clock trees is entirely unrelated to minimizing wire delay.

Applicants respectfully note that similar further patentable distinction is found in each of Claims 14 and 21. With respect to optimization, Claim 14 includes: *"assigning each wire to a layer, and inserting buffers at optimal distances"* and Claim 21 includes: *"minimizing a delay in each wire by inserting*

buffers at optimal distances." Accordingly, Applicants respectfully submit that each of Claims 10, 14, and 21 are yet further patentably distinct over the cited reference.

Applicants respectfully request consideration of dependent Claim 4. Claim 4 recites:

> ***4. The method of Claim 3, wherein performing physical optimization of wire placement further comprises selecting a layer for each wire based on wire length.***

Therefore, in addition to the patentably distinguishing limitations present in parent Claim 1, Claim 4 includes that the optimization of each wire comprises ***"selecting a layer for each wire based on wire length*** " However, *Dupenloup* fails to teach or suggest the same.

Applicants respectfully traverse the assertion in the outstanding Office Action that states *Dupenloup* (at col. 80, lines 13-17) teach selecting a layer for a wire based on wire length. In fact *Dupenloup*'s specification of geometric values (e.g., wire width and layer assignment, at col. 80, lines 15-16) during detailed routing makes no mention of layer selection based on wire length.

Claim 9 includes assigning a wire to *"... a layer based on the relative length of the wire"* and Claim 20 includes *"selecting a layer for each wire based on the wire length."* Therefore, Applicants respectfully submit that each of Claim 4, 9, and 20 find further patentable distinction over and above their respective base claims.

Consequently, no further issues are believed to be outstanding, and it is respectfully submitted that this case is in condition for allowance. An early and favorable action is respectfully requested.

Respectfully submitted,

REED SMITH LLP

Dated: February 10, 2005

By: _____
Name: John W. Carpenter
Registration No. 39,129
Attorney for Applicant

Two Embarcadero Center
Suite 2000
PO Box 7936
San Francisco, CA 94120-7936
Direct Dial (415) 659-5927
(415) 391-8269 Facsimile